IN THE CLAIMS:

Claim 2 has been amended herein. All of the pending claims 1 through 17 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Previously presented) A semiconductor device assembly, comprising:

a carrier substrate including a substantially planar structure, at least one opening formed through the carrier substrate, and at least one first contact area on a first surface of the substantially planar structure, proximate to the at least one opening; and

a solder mask positioned on the first surface, extending to an outer peripheral edge of the first surface, and comprising at least one opening through which the at least one opening and the at least one first contact area of the carrier substrate are exposed.

2. (Currently amended) The semiconductor device assembly of claim 1, further comprising:

at least one semiconductor die secured to a second surface of the carrier substrate opposite the first surface thereof, at least one bond pad of the at least one semiconductor die being exposed through ~~said~~ the at least one opening of the solder mask and the at least one opening of ~~said~~ the carrier substrate.

3. (Previously presented) The semiconductor device assembly of claim 2, further comprising:

at least one intermediate conductive element extending between the at least one bond pad and the at least one first contact area.

4. (Previously presented) The semiconductor device assembly of claim 3, wherein a thickness of the solder mask exceeds a height the at least one intermediate conductive element protrudes above the first surface of the substantially planar structure of the carrier substrate.

5. (Previously presented) The semiconductor device assembly of claim 3, further comprising:

encapsulant material within the at least one opening of the substantially planar structure of the carrier substrate and the at least one opening of the solder mask.

6. (Previously presented) The semiconductor device assembly of claim 5, wherein an upper surface of the encapsulant material is substantially level with an outer surface of the solder mask.

7. (Previously presented) The semiconductor device assembly of claim 5, wherein a distance between an uppermost portion of the at least one intermediate conductive element and an outer surface of the solder mask is at least about 25 μm.

8. (Previously presented) The semiconductor device assembly of claim 7, wherein the at least one intermediate conductive element comprises a bond wire and a thickness of the solder mask is equal to the sum of a distance of a portion of a loop of the bond wire that protrudes above the surface of the carrier substrate and about 25 μm.

9. (Previously presented) The semiconductor device assembly of claim 1, wherein the carrier substrate includes at least one second contact area on the surface thereof and at least one conductive trace electrically connecting the at least one first contact area and the at least one second contact area.

10. (Previously presented) The semiconductor device assembly of claim 9, wherein the at least one second contact area is at least partially exposed through an aperture of the solder mask.

11. (Previously presented) The semiconductor device assembly of claim 10, further comprising:

at least one discrete conductive element protruding from the at least one second contact area above the solder mask.

12. (Previously presented) The semiconductor device assembly of claim 11, wherein at least half of a height of the at least one discrete conductive element protrudes above an outer surface of the solder mask.

13. (Previously presented) The semiconductor device assembly of claim 1, wherein the solder mask comprises a material with a coefficient of thermal expansion substantially the same as a material of the carrier substrate.

14. (Previously presented) The semiconductor device assembly of claim 1, wherein the solder mask comprises a cured photoimageable material.

15. (Previously presented) The semiconductor device assembly of claim 1, wherein a thickness of the solder mask is about 50 μm to about 100 μm.

16. (Previously presented) The semiconductor device assembly of claim 1, wherein the solder mask comprises a plurality of adjacent, mutually adhered regions.

17. (Previously presented) The semiconductor device assembly of claim 1, wherein the solder mask comprises an insulative material.